IN THE CLAIMS

1. (Currently amended) A circuit for reducing standby leakage in a memory unit, comprising:
a capacitive divider coupled to the memory unit so as to generate a voltage across the memory unit, the voltage being adequate to retain memory values during one of a sleep state and a standby state, wherein the memory unit is coupled between Vss and Vddinternal terminals.

2. (Original) The circuit according to claim 1, wherein said capacitive divider is coupled to the memory unit on-chip.

3. (Original) The circuit according to claim 1, wherein the voltage is a division of a normal operating voltage.

4. (Original) The circuit according to claim 3, wherein the voltage is substantially Vdd/2.

5. (Original) The circuit according to claim 3, wherein the voltage is substantially Vdd/3.

6. (Original) The circuit according to claim 1, wherein said capacitive divider is configured for varying an oscillator frequency in accordance with the generated voltage so as to minimize switching losses.

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7-10. (Cancelled)

11. (Currently amended) An inductive circuit for reducing standby leakage in a memory unit, comprising:
an inductive divider coupled to the memory unit so as to generate a voltage across the memory unit, the voltage being adequate to retain memory values during one of a sleep state and a standby state, wherein the memory unit is coupled between Vss and Vddinternal terminals.

12. (Original) The inductive circuit according to claim 11, wherein said inductive divider is coupled to the memory unit on-chip.

13. (Original) The inductive circuit according to claim 11, wherein the voltage is a division of a normal operating voltage.

14. (Original) The inductive circuit according to claim 13, wherein the voltage is substantially Vdd/2.

15. (Original) The inductive circuit according to claim 13, wherein the voltage is substantially Vdd/3.

16. (Original) The inductive circuit according to claim 11, wherein said inductive divider is configured for varying an oscillator frequency in accordance with the generated voltage so as to minimize switching losses.

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17-20. (Cancelled)

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